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If ARPA project, please check below:

INVENTION DISCLOSURE

___ Advanced SRAM
___ BST
___ FED
___ FE RAM
___ NCAICM

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Exhibit A
09/434,082
Declaration under 37CFR1.131

1. INVENTOR(S): Kevin J. Ryan

2. DESCRIPTION

2.1 Title of invention: Packet-Oriented Synchronous DRAM Bus Interface

2.2 Brief description: A synchronous DRAM interface consisting of a control/address bus and a separate data bus, intended to facilitate either narrow or wide bus implementations, and to improve performance over existing packet-oriented DRAM technologies.

2.3 Also attach a complete description, including drawings or sketches and articles relevant to the invention. Legible photocopies of laboratory notebooks are acceptable.

See attached.

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3. INFORMATION CONCERNING CONCEPTION OF INVENTION

3.1 CONCEPTION AND DOCUMENTATION OF THE INVENTION

a. Identify the date when you first conceived the invention. (If not sure, give the earliest date of which you are sure.)

b. To whom was the idea first described and on what date? (Other than a co-inventor.)

Terry Walther on :

c. Identify the date of the first tangible record such as computer simulation, tape out, drawing or written description. Please specify type and location.

3.2 CONCEPTION OF THE INVENTION

a. Please identify related invention disclosures, patents or other publications describing similar ideas, and other companies working in the same field. Attach copies, if available.

Other companies working in the same field include DRAM vendors, DRAM users such as Intel, and third parties such as RAMBUS.

b. What is the closest technology, of which you are aware?

RAMBUS RDRAMs, SDRAMs.

c. Identify the advantages of this invention over previous technology.

The proposed solution provides for narrow bus implementations when cost and or granularity issues are of primary importance, or for efficient wide bus implementations where performance is more important than granularity. In contrast to RAMBUS, complete additional independent channels do not need to be added in order to increase data bus width. Also in contrast to RAMBUS, the pipelining or overlapping of operations is facilitated by separating the command/address bus from the data bus, thus avoiding the arbitration and associated performance degradation resulting from sharing one bus. (In other words, with this invention, subsequent commands may be issued while data from a previous command is occupying the data bus, with RAMBUS this is not true.)

3.3 IMPORTANT DATES

a. Has the invention been disclosed outside the company? NO If yes, to whom, when, and in what form?

b. Have any articles describing your invention been published? NO If yes, list author(s), title of article, publication and date.

c. Have any engineering samples been given out? NO If yes, to whom and on what date?

d. Has any product using the invention been sold or offered for sale? NO If yes, to whom and on what date?

3.4 DISPOSITION OF THE INVENTION

a. When will (or did) Micron begin use of the invention experimentally? Has not yet; to be determined.

b. When will (or did) Micron begin production of this invention? Has not yet; to be determined.

3.5 MISCELLANEOUS INFORMATION

a. Was the invention developed during a joint development agreement or other contract with an outside company? NO

b. Please list developmental work outside of the company (including Government proposal or contract).

None.

4. INVENTORS:

Name: Kevin J. Ryan
Micron Phone: 368-3954 Micron Mail Stop: 607

Company Name(VERY IMPORTANT): Dept. Name: Marketing
___ Micron Semiconductor, Inc. Dept. #: 950H
___ Micron Computer, Inc.
___ Micron Custom Manufacturing Services, Inc.
___ Micron Display Technology, Inc.
___ Micron Communications, Inc.
_x_ Other Micron Technology, Inc.

Home Address: 508 E. Kingsford Dr.
Meridian, ID 83642

Citizenship: USA

Supervisor: Brett Williams

Signature: _____ Date:

5. WITNESS

If there is only one inventor, a witness should sign and date this disclosure. A witness in this case is a non-inventor who understands the nature of the invention.

_____
(Signature of Witness)

Notebook # 0100548

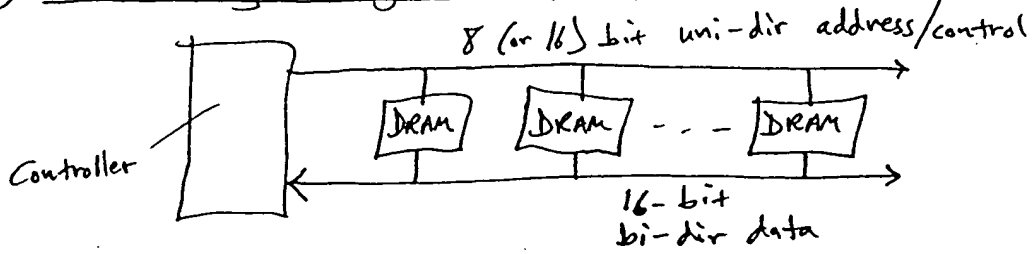
Project Number Subject SyncLink Date

The most promising SyncLink configuration is one where there is either an 8-bit or 16-bit input bus to the DRAMs (for address and control info) and a 16-bit bi-directional data bus.

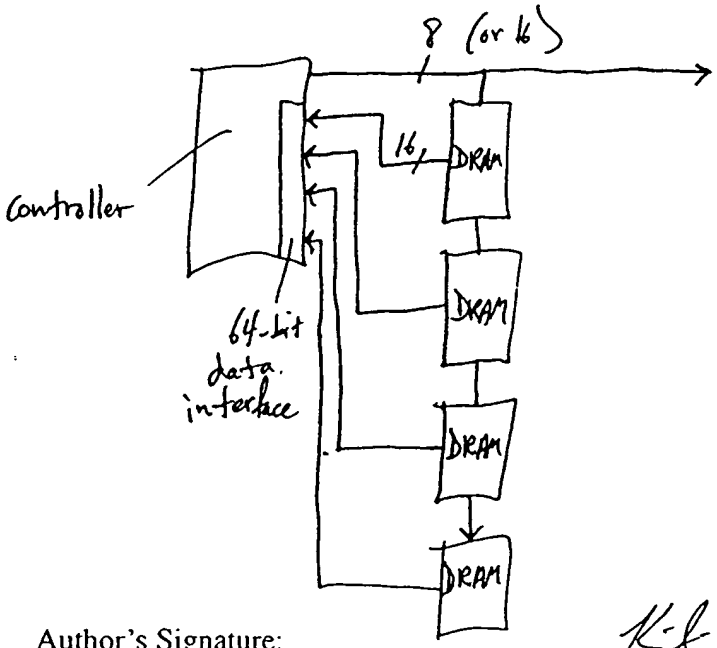
The system can be expanded in depth by adding DRAMs to this 16-bit data channel, or in width by adding more 16-bit data channels. Either way, the input bus goes to all DRAMs in the system.

This is superior to RAMBUS because RAMBUS requires that the control lines be replicated as well when expanding in width.

(A) Optimizing for granularity:



(B) Optimizing for bandwidth:



Please do not write in the margin

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Witness' Signature: _____ Date: _____

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Ideally, tradeoff points between (A) and (B) would be supported to allow for system differentiation.

(A) is attractive if "the granularity problem" comes to be. Then OEMs could build a system containing 1 DRAM device (4M x16 at the 64M level) and get a minimum configuration and granularity (8 MBytes).

(B) is attractive if the granularity problem does not come to be.

(A) is therefore a RAMBUS alternative, so the protocol in this case should be superior to RAMBUS and the physical environment should be as good or better.

(B) should compete vs. both SDRAM and a width-expanded RAMBUS in both protocol and physical performance. Since the arrangement is logically similar to the SDRAM bus, the performance improvement is likely to come from limiting the number of module sockets, the number of loads per socket, and defining the signal swings and termination, etc.

In either case, we will probably want to support at least one socket on each channel. The controller and at least one device per channel will probably be soldered down on the motherboard.

Need to define max # of devices per module. Also come up with scheme to allow for a second user upgrade that does not require the user to remove and discard a previous upgrade (especially in a single socket case).

Can we define a stackable module, with or →

Author's Signature: K. J. L Date: _ _

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without a dummy load plug ?

Investigate the main causes of speed degradation in SDRAM module based systems and rectify. All physical improvements will apply to SDRAM based systems as well, so protocol must be superior.

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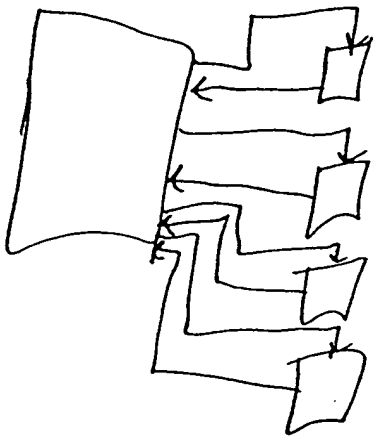
Considering RAMBUS in configurations (A) + (B) on page 7:

First, (B) would have to be modified as follows



because RAMBUS requires that the entire channel (31 pins) be replicated for width expansion.

A clearly more attractive alternative would be to only replicate the data pins. In addition to the physical advantage (fewer pins and traces, etc.) the protocol becomes more efficient (overhead remains the same, in MB/s, while bandwidth increases, as opposed to increasing along with the bandwidth, as it does for RAMBUS).

So clearly, separating the data from the address and control is attractive. SDRAM already does this, so how can we improve on SDRAM?

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Witness' Signature: _____ Date: _____

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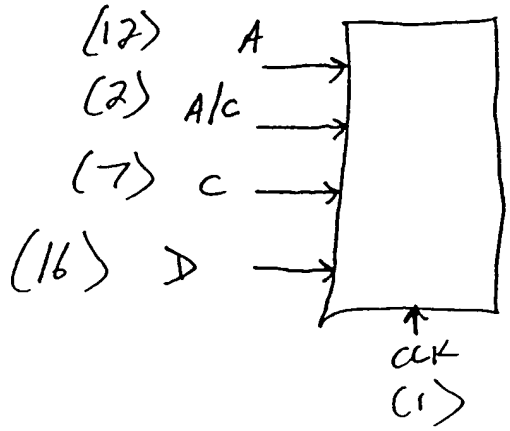
Consider a 4M x 16 SDRAM:



A = Address Only

A/C = Muxed Address + Control

C = Control Only

D = Data

Control = RAS, CAS, WE, CS, CKE, DQML, DQMH

It has 21 control/address pins, so clearly there is a physical advantage to reducing this to 8 or 16 and multiplexing the same information. To provide a performance/efficiency advantage, some degree of scheduling ~~would~~ might have to be provided to offset the latency involved with multiplexing this information.

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